



Inventors: Jingsong XIA et al.
Error Generation for Adaptive Equalizer
Attorney Docket No. 31075-6

FIGURE 1

100

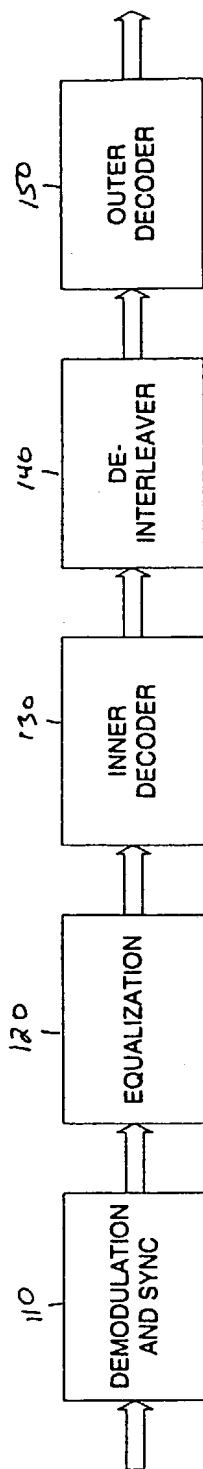
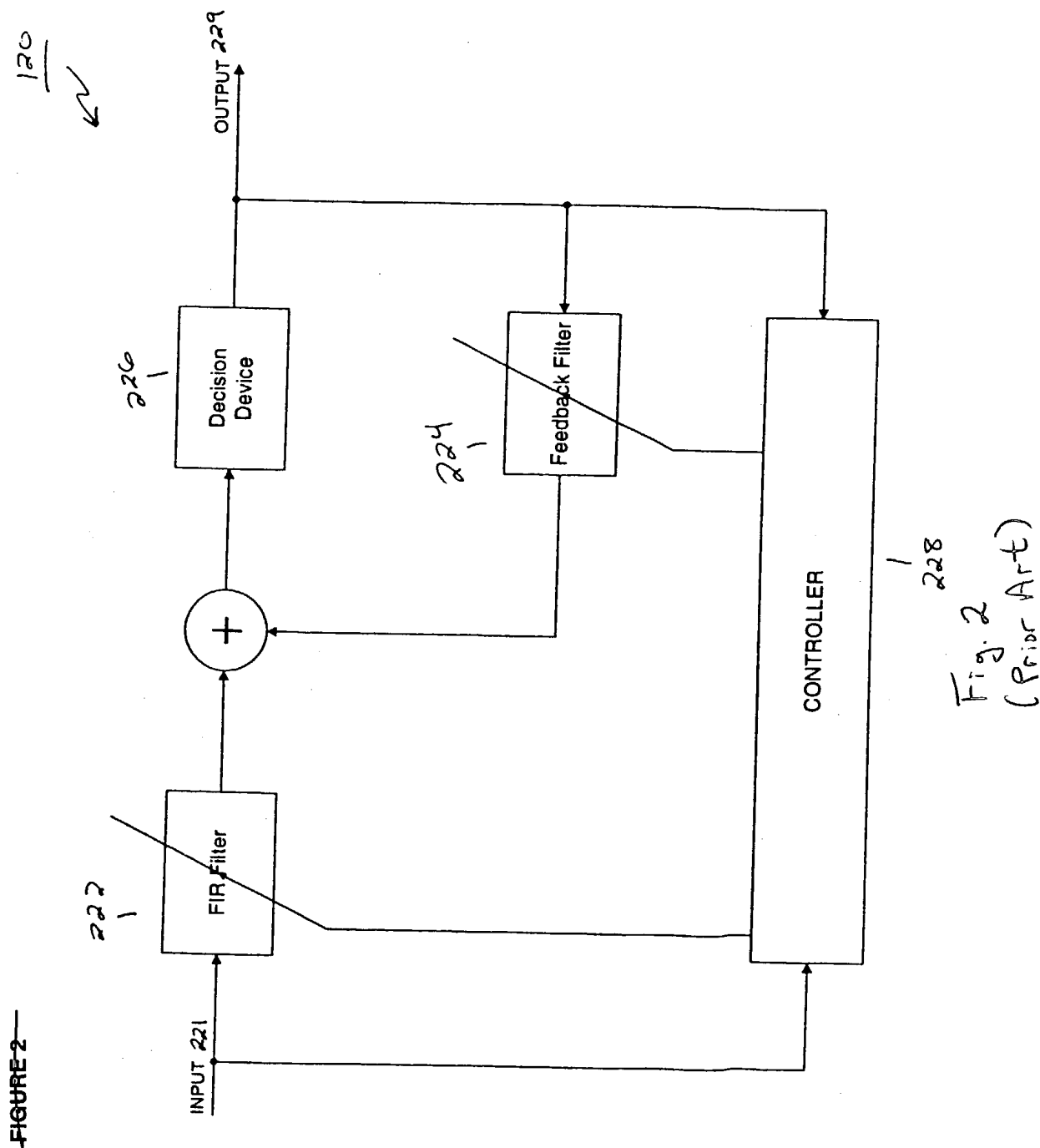


Fig. 1
(Prior Art)



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Serial No. 09/876,547
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FIGURE 3

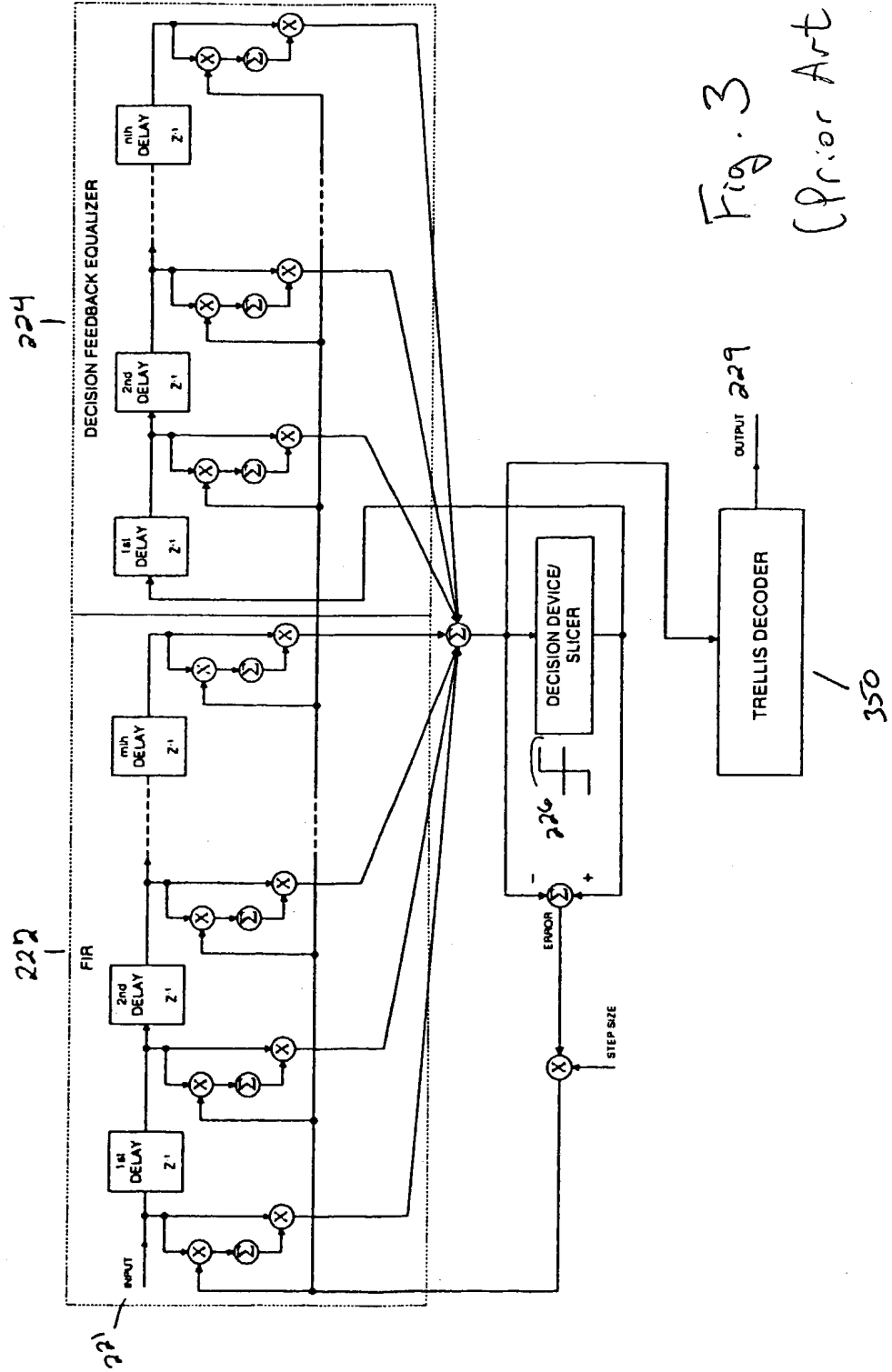
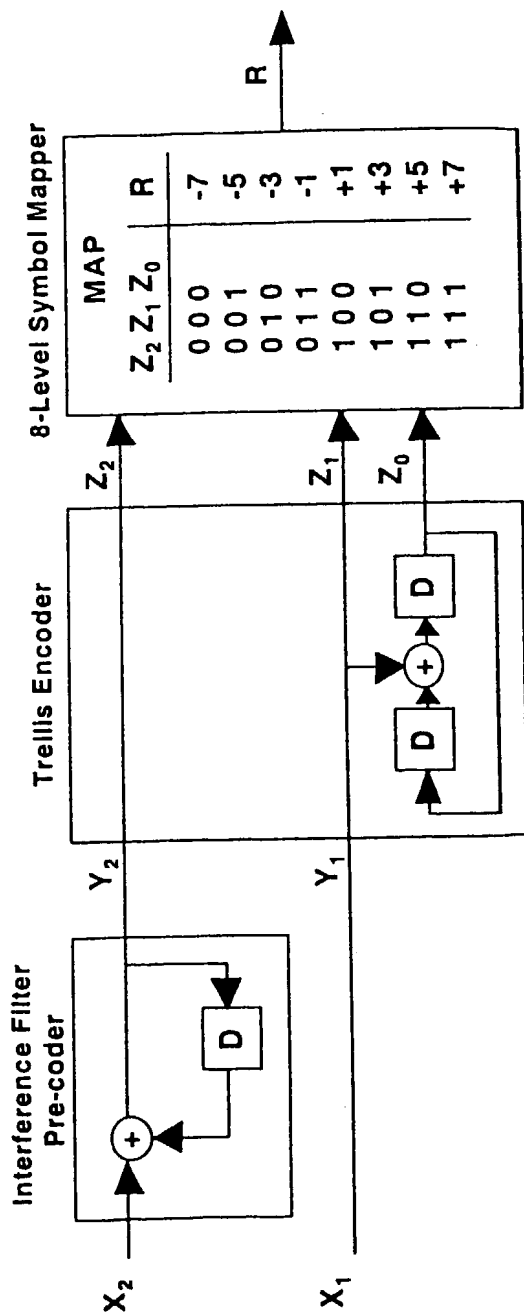


Fig. 3
 (Prior Art)



FIGURE 4

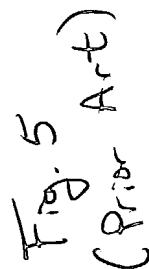
400
N



(D = 12 Symbols Delay)

Fig. 4
(Prior Art)

005





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FIGURE 6

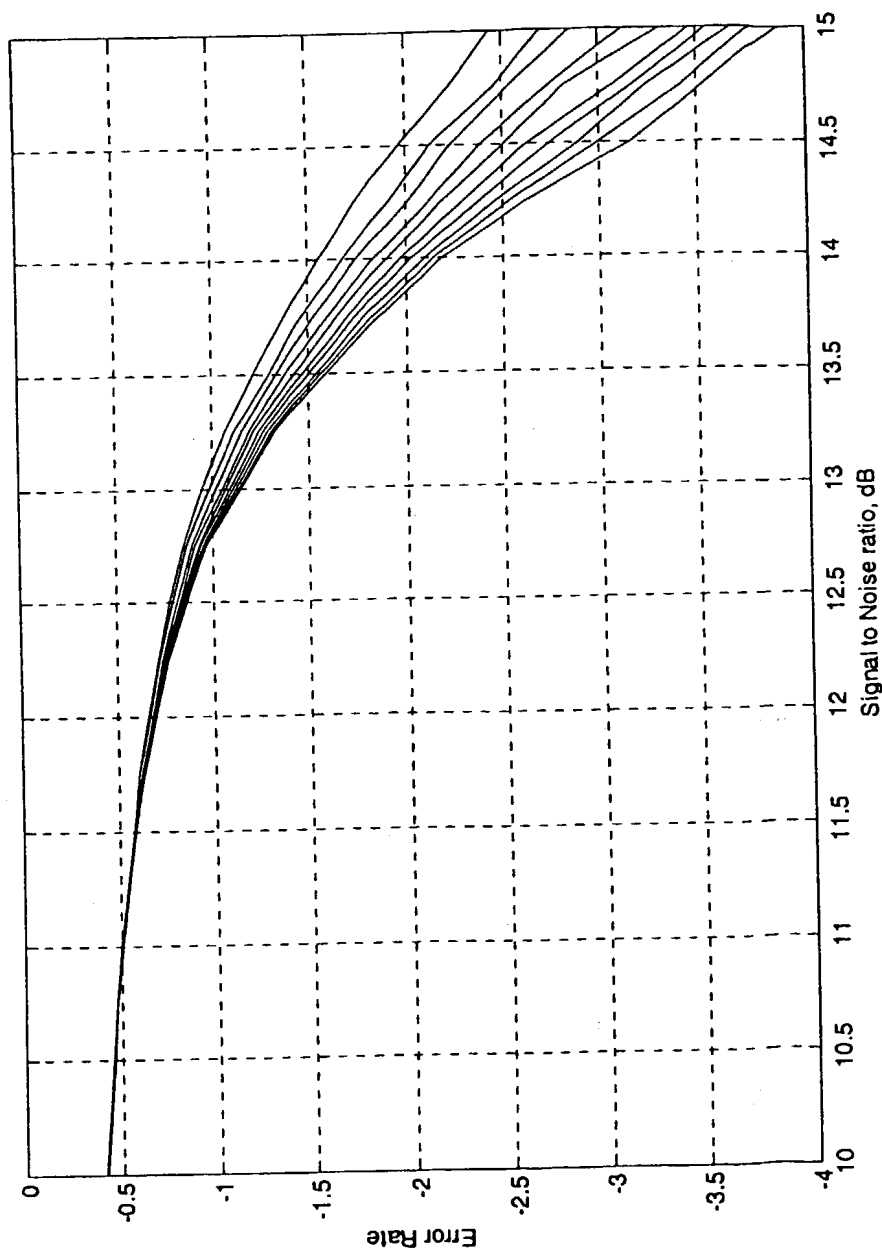


Fig. 6
(Prior Art)



FIGURE 7

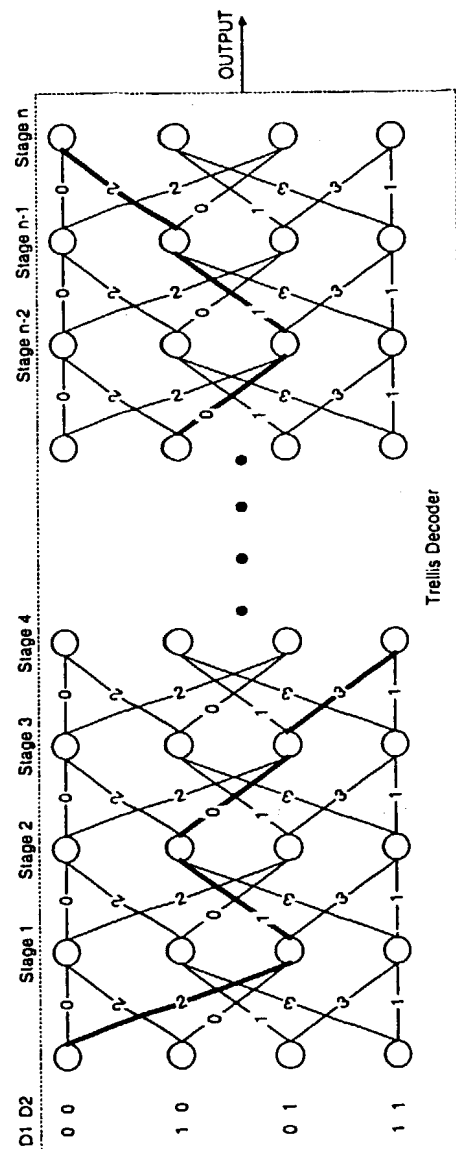
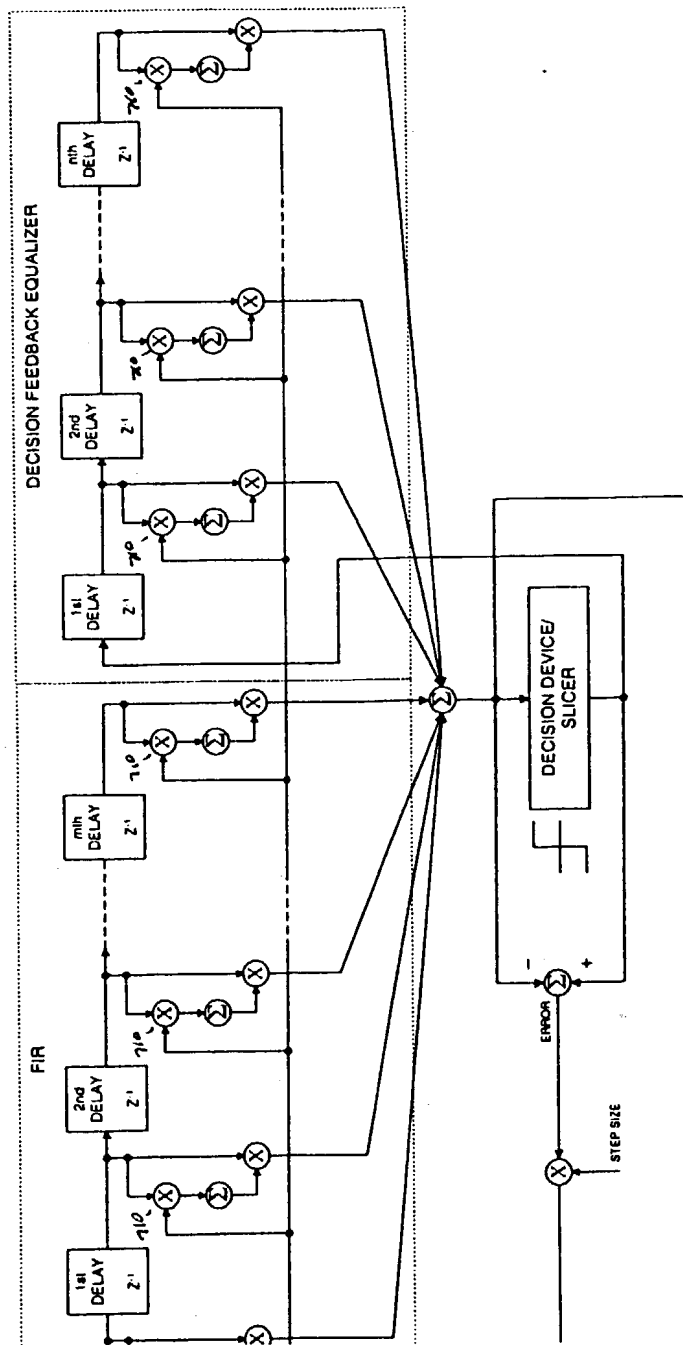
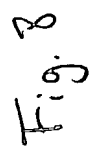


Fig. 7
(Prior Art)

058



~~FIGURE 8~~

OS

222

The diagram illustrates a trellis decoder system with the following components and connections:

- Inputs:**
 - 224:** A handwritten label for the input signal entering the FIR section.
 - 320:** A handwritten label for the **STEP SIZE** input.
- FIR Section (Left):**
 - Contains a **1st DELAY z^{-1}** and a **2nd DELAY z^{-1}** .
 - Each delay stage is followed by a multiplier (\times) and an adder (\oplus).
 - Handwritten label **222** is placed above the FIR section.
- Decision Feedback Equalizer (FBE) Section (Middle):**
 - Contains a **1st DELAY z^{-1}** , a **2nd DELAY z^{-1}** , and a **3rd DELAY z^{-1}** .
 - Each delay stage is followed by a multiplier (\times) and an adder (\oplus).
 - Handwritten label **224** is placed above the FBE section.
- Summing Junction:**
 - Receives inputs from the FIR section and the FBE section.
 - Output is labeled **350**.
- Decision Device / Slicer:**
 - Receives the signal from the summing junction.
 - Output is labeled **360**.
- Delay C:**
 - Receives the signal from the Decision Device / Slicer.
 - Output is labeled **370**.
- Error Calculation:**
 - The signal from **370** is subtracted (\ominus) from the **STEP SIZE** input (**320**) at an adder.
 - The result is labeled **910**.
- Mapper:**
 - Receives the signal from the error calculation adder.
 - Output is labeled **920**.
- Trellis Decoder:**
 - Receives the signal from the Mapper.
 - Output is labeled **930**.
- Final Output:**
 - The signal from the Trellis Decoder is labeled **940**.

15